DEVELOPMENT OF SURFACE ACOUSTIC WAVE DEVICES IN ZnO/SOI SUBSTRATES

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Abstract
Surface acoustic wave is sensitive to the surrounding environment. Wave amplitude and frequency can be used to build various types of S.A.W. based sensors. Of particular importance is the development of S.A.W. based smart sensors. Smart sensors is a class of devices which the sensing element is integrated with the necessary electronics on the same chip. However, as silicon is not a piezoelectric material, it is necessary to develop a compatible piezoelectric thin film technology. Silicon On Insulator (SOI) wafers have become an important substrate for the development of low power, high frequency circuits. We report on the development of a compatible piezoelectric thin film technology on SOI wafers.

Keywords: SAW, SOI, Sensors

1. INTRODUCTION

Surface Acoustic Wave (S.A.W.) devices have gained widespread use since its introduction in the mid 60's[1,2]. It has found application in many areas, such as: radar, frequency hoping, signal processing, frequency multiplexers, etc. One such area is the sensor industry[3]. Much effort has been developed to understand the behaviour of surface acoustic wave devices in a liquid environment[4-6]. For such application is desirable to integrate the SAW device with the necessary electronics. Integration allows for the development of acoustic devices combined with the necessary signal processing circuitry, all on the same chip[7]. This is known as S.A.W. based smart sensors.

Silicon integrated circuit (I.C.) technology is a mature, well developed technology. As silicon is not piezoelectric material, is necessary to develop a compatible piezoelectric thin film technology to combine SAW devices with silicon integrated circuitry. We report on the development of a compatible piezoelectric thin film technology. The film composition is zinc oxide (ZnO), which is piezoelectric if the deposited film is polycrystalline. The deposition is done on silicon on insulator (SOI) wafers, which is an emerging substrate for low power, high frequency circuits[8]. SOI wafers has an embedded silicon oxide layer, which may act as an etch stop for micromachining[7]. The buried oxide isolates the circuitry on the top silicon layer.

2. FABRICATION

The designed process flow is as follows. The starting substrate is a single crystal Si(100) SOI wafer about 300μm thick, the buried oxide is 2000A below the surface, and is 4000A thick. After cleaning, the wafer is placed in the sputtering chamber for the deposition of the zinc oxide thin film. Zinc oxide in its crystalline form is a tetrahedron structure with an oxygen atom at the center. It is a piezoelectric crystal and can be deposited as a polycrystalline thin film. Some key material parameters for zinc oxide thin film is presented in Table I.

Table I. Material parameters for ZnO-thin film[9].

	v (m/s)	K^2 (%)	TCD (ppm/^{o}C)
ZnO-thin film	5160 - 5500	4.5 - 6.0	40 - 43

In the sputtering chamber a high purity zinc target is placed in contact with an oxygen/argon plasma; the zinc atoms sputtered from the target deposit as zinc oxide onto the substrate. By controlling RF power, substrate temperature and the argon to oxygen ratio is possible to deposit high quality polycrystalline ZnO thin films (some typical process parameters is presented in Table II). Film quality can be determined by X-ray diffraction.

Table II. Process parameters for the fabrication of ZnO-thin films.

Target	Zn (99.999%)
D.C. power	1.5kW (500V, 3A)
Oxygen pressure	0.9kPa
Substrate temperature	375^{o}C
Target-substrate spacing	15cm
Sputter time	5-10min
Sputter rate	~1000 A/min

The next step is to fabricate the InterDigiTal (IDT) structure. This structure consists of two comb structures opposite to each other. First, a metal film is deposited by thermal evaporation or electroless technique and a layer of photoresist is spun-on. After exposure, the photoresist is developed and the metal etched to form the IDT structure. Acetone is used to remove the remaining photoresist and the device is ready for electrical measurements (see Figure 1).

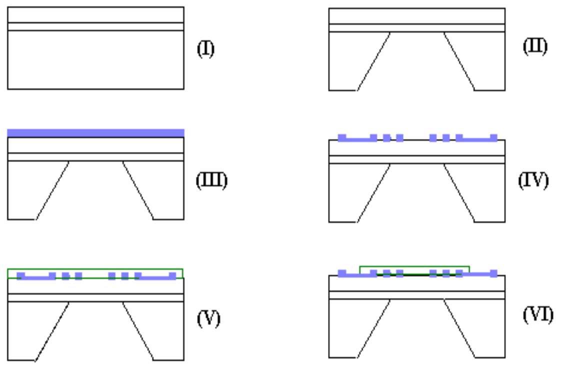

Fig 1 - Fabrication steps: (I) SOI wafer; (II) KOH backside etch; (III) Aluminum evaporation; Lithography for IDT pattern transfer; (V) ZnO sputtering; (VI) Lithography for via opening.

Another possibility is fabricate the IDT structure first and then deposit the ZnO layer. The process flow is illustrated on Figure 1. One important advantage of the ZnO on top is that it may also act as passivation layer for the IDT structure. The final structure schematic is presented in Figure 2.

3. RESULT AND DISCUSSION

The backside etch is done with KOH, and is currently under development, a preliminary result is shown in Figure 3.

Zinc oxide thin film is reported to have a high coupling coefficient, much higher than its crystalline counterpart[9], and its temperature coefficient is smaller than that of lithium niobate. To check the designed SAW comb structures, test devices were fabricated on lithium niobate (see Figure 4). The IDT masks were designed with the Magic Layout Software and was fabricated by CTI. The designed IDT structures have wavelengths of 120microns and 80microns. The frequency response was measured with a network analyzer and the devices operated as predicted with center frequency of 32MHz and 48MHz respectively. The SAW speed can be calculated from:

$$\lambda \cdot f = v$$

This results on a speed of 3840m/s in both cases, which is the expected speed for $LiNbO_3$[11].

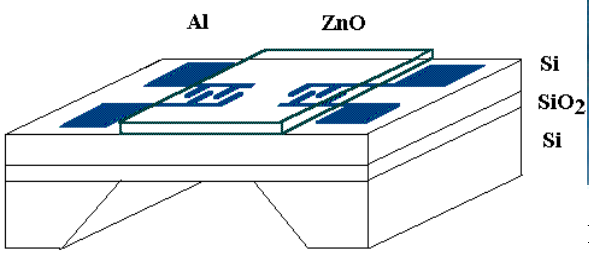

Fig 2 - Final structure schematic.

Fig 3 KOH etch of silicon [10]

The experimental arrangement is shown in Figure 5. It consists of a network analyzer and the device under test. An amplifier is added in closed loop to build an oscillator. The measurement of oscillator frequency change as a function of mass loading will be used to characterize the sensor. It is expected that the amplifier can be integrated with the sensor structure[12].

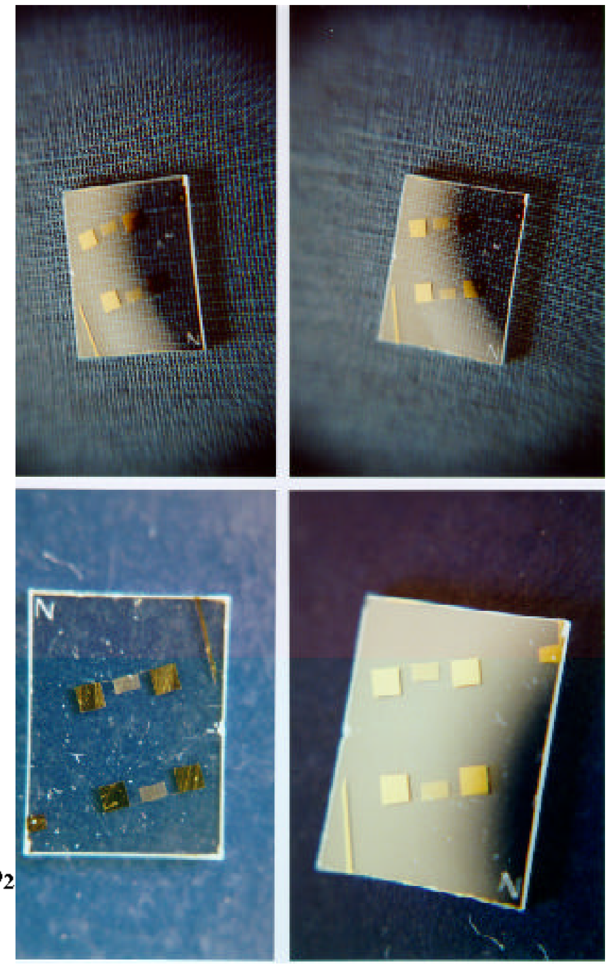

Fig. 4. Example S.A.W. devices fabricated on crystalline substrate to test the IDT comb structure.

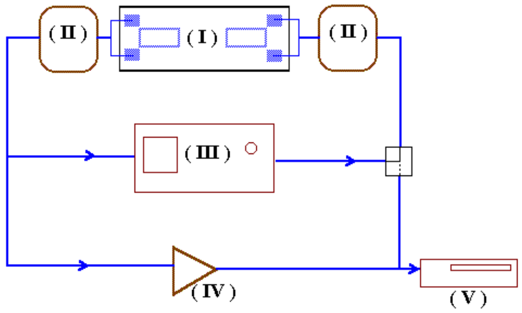

Fig. 5. (I) SAW under test; (II) Matching network; (III) Network Analyzer; (IV) Amplifier; (V) Frequency counter.

4. CONCLUSION

SOI technology[4] presents an alternative to the development of low power, low voltage circuitry for the portable systems industry. The combination of SOI technology with sensor technology, here represented by the surface acoustic wave device, presents an opportunity for the development of a new class of smart sensors. The SAW based sensor is currently under development, the next step will be to integrate some electronics on the same wafer. It is expected that this sensor will have applications in the medical and chemical industries, to name just two key niches.

5. References

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