Numerical Analysis of the Stub Transistor

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Stubbed waveguides and stub transistors are candidates for next generation electronic devices. In particular, such structures may be used in spintronics-based quantum computation, because of its ability to induce spin-polarized carriers. In this paper, we present the simulation of the conductance of the stub transistor (single and double-gated), modeled with a nearest-neighbor tight-binding Hamiltonian. The oscillatory behavior of the channel conductance with the applied stub voltage is observed.

Keywords: mesoscopic, stub transistor, simulation.

I. INTRODUCTION

Many devices are being proposed to substitute the MOSFET, as microelectronics reaches the nanoscale. Among them are the stubbed waveguide and the stub transistor [1, 2, 4, 5, 6, 7]. The stubbed waveguide consists of a nanowire with a set of periodically spaced stubs. The stub transistor is a nanowire with an electric potential applied to the stub, which acts as a gate voltage, see Fig. 1. Such devices can be fabricated with dimensions below $100nm$, which, at low temperatures, is smaller than the length scale over which the electron preserves its phase coherency. This length is known as the electron phase-coherence length, L_ϕ, and the transport through the device is ballistic. These kind of structures are classified as mesoscopic systems and cannot be described by the usual semi-classical transport theory, the wave nature of the electron needs to be taken explicitly into account.

The conductance, G, of the stub transistor displays an oscillatory behavior, as the electric potential applied to the stub, V_G is varied. Therefore, the channel can be opened and closed. A minimum of G is a reflection resonance or antiresonance and a maximum of G is a transmission resonance or just resonance [4]. The transmission zeroes occur as function of the length of the stub, L_{stub}, given by $kL_{stub} = n\pi$, and the resonances are given by $kL_{stub} = (n + 1/2)\pi$. The use of multiple periodically placed stubs transforms the transmission zeroes in blocked transmission bands [4]. Such devices have been fabricated on GaAs/AlGaAs by MBE [6].

To understand the behavior of the device, many theoretical techniques have been used, such as, the recursive Green function technique [2] to calculate the scattering matrix, the transfer matrix technique [4, 7]. Santos [8] has developed a recursive Green function program to simulate ballistic quantum devices.

The reason for the great interest in the stub transistor is the potential for ultrafast signal processing without giving prohibitive energy dissipation. The traditional FET transistor works using a "brute" force switching voltage, because the electric field has to deplete electrons under its gate to change the conductance. The quantum interference devices, QIDs, on the other hand, work by changing the electron interference pattern. This quantum phenomenon requires a lower switching voltage, therefore a lower energy dissipation. The reduced size of the QIDs decreases the time that the electron takes to travel through it, as a consequence, its switching frequency can be increased up to the terahertz frequency region [9].

Strong analogies exist between ballistic quantum devices and similar devices in optics and microwave engineering. One, however, has to take care when try to implement optical or microwave devices using matter electronic waves. These analogies are not perfect because electrons interact strongly and obey Fermi statistics, while photons are bosons.

In this paper, the quantum stub transistor is examined by applying the recursive Green function technique. The paper is divided in five sections, this introduction is the first, next the quantum stub transistor is described. Third an overview of the simulation method is presented. Next, the results and analysis are presented. Finally, the conclusions.

II. THE QUANTUM STUB TRANSISTOR

A schematic view of the quantum stub transistor is shown in Fig. IV, where V_G is the gate voltage and V_D is the drain voltage. The drain voltage is related to the incident electron energy by $E = eV_D$. If the stub length, L_{stub}, is much larger than the inelastic mean free path L_{ine}, then this structure represents just two intersecting wires and the transconductance, $g_m = \partial I_D/\partial V_G$ is zero, where I_D is the drain current. For $L_{stub} \leq L_{ine}$, however, the quantum nature of the electronic transport makes the transconductance g_m different from zero and the situation changes completely. What happens is similar to the conventional metal waveguide, where one has to move a piston inside a

cavity to change the interference patterns of the electromagnetic field. In the case of the quantum stub transistor, the gate voltage acts as a piston by varying the length of the stub. This changes the penetration of the electron inside the stub, and therefore the interference pattern. To represent this change of the stub length with the gate voltage, L_{eff} is defined. The stub length L_{stub} for which quantum effects become important vary widely depending on temperature and material used. In ultra-pure semiconductor material and at liquid Helium ($4.2K$) temperatures and below, coherent effects are observable over distances of $1\mu m$ [3].

The confinement of the propagating electrons from source to drain in the transverse direction allows only discrete energy levels or modes. The number of transverse modes, M, for a quantum stub transistor with width W is given by the ratio between the width and the Fermi wavelength, λ_F, as shown in Equation 1.

$$M = Int\left(\frac{W}{\frac{\lambda_F}{2}}\right) \tag{1}$$

where $Int(x)$ represents the integer that is just smaller than x.

If more than one mode propagates through the device, each mode will have a different penetration length in the stub, as a consequence the device will display an erratic interference pattern. Hence, for a well behaved device the incident energy, E, must be in the range $E_1 \leq E < E_2$, where E_1 and E_2 are the energy of the first and second mode respectively. The energy of the n-th mode can be estimated with the infinite potential box approximation.

$$E_n = \frac{\hbar^2}{2m^*}\frac{n^2\pi^2}{W^2} \tag{2}$$

where m^* is the electron effective mass.

The electron may follow many different paths, as it propagates through the device. The maximum length difference occurs between a path going straight from source to drain and another going through the stub and then to the drain. This difference is approximately $2L_{stub}$. So the number of minima expected in the interference pattern is $m+1$, where m is the maximum integer that satisfies the inequality below

$$L_{stub} \geq (m + \frac{1}{4})\lambda_F. \tag{3}$$

For example, for $L_{stub} = 30nm$ and $\lambda_F = 20nm$, one gets $m + 1 = 2$.

III. THE SIMULATION METHOD

To simplify the analysis, it is assumed that the potential inside the device is equal to zero, and the borders of the device are defined by a high potential barrier. Even with these simplified boundary conditions, the two dimensional nature of the devices makes the problem of finding the total transmission probability, T, of the electron through the device, analytically intractable. To obtain the conductance of the device using the Laudauer formula ($G = \frac{2e^2}{h}T$), it is necessary to use a numerical method to solve Schrödinger equation ($H\Psi = E\psi$). Hence, the geometry has to be described with a model Hamiltonian, this is done, by using the nearest-neighbor tight-binding model. To implement such model, the structure showed in Fig. IV is filled with a sufficient dense square lattice with periodicity a. The plane wave motion can be emulated by a tight-binding Hamiltonian, when the lattice parameter, a, is much smaller than all other length scales of the problem. Proceeding as indicated, one may reasonably expect to correctly reproduce the continuous dynamics.

To better illustrate the method, an example of a square lattice is shown in Fig. IV. Each slice is stored as a column of the device matrix, where the matrix entry is related to the potential energy confining the electron. Each column (slice) of the device matrix is used to construct the Hamiltonian or slice matrix for numerical calculation by using the tight-binding Hamiltonian Model. The nth slice matrix is shown in Equation 4.

$$H_n = \begin{pmatrix} V_1 - 4t & -t & 0 & ... & 0 \\ -t & V_2 - 4t & -t & ... & 0 \\ 0 & -t & V_3 - 4t & ... & 0 \\ . & . & . & & . \\ . & . & . & & . \\ . & . & . & & . \\ 0 & 0 & 0 & ... & V_M - 4t \end{pmatrix} \tag{4}$$

where V_i in the diagonal is the local potential energy profile at a given slice, and t is a coupling term, given by Equation 5.

$$t = E_F \left(\frac{1}{2\pi}\right)^2 \left(\frac{\lambda_F}{a}\right)^2 \tag{5}$$

where E_F is the Fermi energy level.

The Schrödinger equation is now solved by using the Green function method, i.e., the equation to the solved has the form:

$$(E\underline{I} - \underline{H})\underline{G} = \underline{I} \tag{6}$$

where $\underline{I}$ is the identity matrix, and $\underline{G}$ is the Green function matrix. For simulations with practical interest, the direct inversion of the matrix $(E\underline{I} - \underline{H})$ requires huge amounts of memory and processing power. This is circumvented by employing an iterative method for the computation of the Green function. The details of the program can be found in Reference [8].

The data input process is time consuming, as the device has to be described in matrix format. To facilitate data input, a front-end that converts the device geometry from a standard bit-mapped format into the matrix format that the computation algorithm understands has been developed [10]. The relation between the width W of the device and the number of pixels P_W used to represent this dimension is given by

$$W = (P_W + 1)a. \tag{7}$$

For $a = 0.5nm$ and $W = 10nm$, $P_W = 19$.

IV. RESULTS AND ANALYSIS

The program uses normalized units, E_F is the unit of energy and $2e^2/h$ is the unit of conductance. In the simulations, it is assumed that the gate voltage, V_G, drops linearly along the stub[11]. The effective mass is $m^* = 0.07m_0$ (GaAs), the wire width is $W = 10nm$ and the lattice parameter is $a = 0.5nm$.

The normalized coupling term is calculated with Equation 5. Considering the single mode device, $t = 40.52$. Using an incident energy equal to the first allowed mode $E_1 = 53meV$, the plot of the conductance as a function of the normalized incident energy is presented in Figure IV. The result confirms that the device has only one mode. The gate voltage is set equal to zero, $L = 73.3nm$ and $L_{stub} = 11nm$.

Considering now a device with four open transmission channels, the simulation yields a conductance with interference patterns, at each conductance step [6]. The plot of the normalized conductance as a function of the normalized incident energy is presented in Figure IV. For this simulation, $W = 10nm$, $P_W = 19pixels$, $L_{stub} = 50nm$, $M = 4$ (four modes), and $t = 2.533$.

Next, the incident energy (drain voltage) is fixed at a position to get just one open channel, and the gate voltage is varied. The normalized conductance as a function of the gate voltage are presented in Figure IV and IV. The results show that the conductance varies between one and zero, as the gate voltage varies. In Figure IV, there are two conductance dips or antiresonances (zero conductance). In Figure IV, there are three antiresonances. This can be used to test the correctness of Equation 3, two values L_{stub} are used. For this calculation, the incident energy is $53meV$ and $\lambda_F = 20nm$. Hence, for $L_{stub} = 29nm$, one gets $m = 1$, and the number of minima is $m + 1 = 2$. For $L_{stub} = 50nm$, one gets $m = 2$, and the number of minima is $m + 1 = 3$. The calculated number of minima are in accordance with the simulation.

Another configuration is the gate-all-around stub transistor. This transistor has a double stub, one opposite to the other. The calculated conductance as a function of the gate voltage is presented in Figure IV. The presence of the gate-all-around stub narrows the antiresonance.

These are interesting results, because one can control the channel transmission, by applying a control voltage, which is useful in digital logic, for instance. The main practical difficulty is that the width of the antiresonance is very narrow, and one would have to set the voltage with great precision. However, It is known that in a stubbed waveguide the presence of a series of stubs transforms the antiresonance in blocked bands [4]. The idea is to increase the number of stubs to get a wider blocked transmission band. The simulation is now carried out varying the number of stubs along the device. The double stub transistor is shown in Figure 8. The result, presented in Figure 9, shows that the antiresonance is replaced by double antiresonances. By adding three stubs, one gets a triplet. Therefore, increasing the number of stubs may be a practical solution for the realization of stub transistors, as the blocked transmittance gets less sensitive to a particular gate voltage level.

Conclusions

Besides the potential for high-speed operation, the appeal of the quantum stub transistor is its very small dimensions and the possibility of operation at very low power levels, which could allow extremely high-level of integration. But, as pointed by Laundauer, like the others (QIDs), this kind of device requires very specific values of the control signal and of the devices parameters for a conductance maximum or minimum. This leaves little room for device fabrication errors. However, the results in this paper show that the use of multiple stubs reduces this problem by widening the antiresonance. This may be a reasonable approach for the practical realization of stub transistors.

Acknowledgments

The authors would like to acknowledge the support of CNPq under the "Instituto do Milênio" Initiative.

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[1] F. Sols,M. Macucci, U. Ravaioli, and K. Hess, "On the possibility of transistor based on quantum interference phenomena" *J. Apply. Phys.,* **vol. 54** , 350-352 (1988).

[2] F. Sols,M. Macucci, U. Ravaioli, and K. Hess, "Theory for quantum modulated transistor" *J. Apply. Phys.,* **vol. 66** , 3892-3906 (1989).

[3] T. Palm, L. Thylen, O. Nilsson, and C. Svensson, "Quantum Interference devices and field-effect transistors: A switch energy comparison," *J. Apply. Phys.,* **vol. 74, no 1** , 687-695 (1993).

[4] P. Singha Deo, A. M. Jayannavar, "Quantum Waveguide Transport in Serial Stub and Loop Structures," *cond-mat/9411028 and Phys. Rev. B* 50 (16): 11629-11639 (1994).

[5] P. Singha Deo, M. V. Moskalets, "Features of level broadening in a ring-stub system," *cond-mat/9909403 and Phys. Rev. B* 61 (16): 10559-10562 (2000).

[6] P. Debray, O. E. Raichev, P. Vasilopoulos, M. Rahman, R. Perrin, W. C. Mitchell, "Ballistic electron transport in stubbed quantum waveguides: experiment and theory," *cond-mat/0002284 and Phys. Rev. B* 61 (16): 10950-10958 (2000).

[7] X. F. Wang, P. Vasilopoulos, F. M. Peeters, "Spin-current modulation and square-wave transmission through periodically stubbed electron waveguides," *cond-mat/0204415 and Phys. Rev. B* 65, 165217 (2002). X. F. Wang, P. Vasilopoulos, F. M. Peeters, "Ballistic spin transport through electronic stub tuners: spin precession, selection, and square-wave transmission," *cond-mat/0204391 and Appl. Phys. Lett.* 80, 1400 (2002).

[8] Edval J. P. Santos, "Simulation of the DC conductance of ballistic quantum devices," in *Proceedings of the SBMicro 2002*, N. I. Morimoto, R. P. Ribas, R. Verdonck, Editors, PV2002-8, p. 56-62, The Electrochemical Society Proceedings Series, Pennington, NJ (2002).

[9] V. V. Mitin, V. A. Kochelap, and M. A. Stroscio, in "*Quantum heterostructures: microelectronics and optoelectronics*," Chapter 9, pp. 393, Cambridge University Press, Cambridge (1999).

[10] Alexandre B. Guerra and Edval J. P. Santos, "CAD front-end for nanodevice design" in *Proceedings of the II Students Forum on Microelectronics,* Porto Alegre, RS (2002).

[11] The program does not have a Poisson solver for the calculation of the gate potential distribution, this feature will be added in the near future.

Figure captions

Fig. 1. Schematic view of the quantum stub transistor, where V_G is the voltage applied to the stub, V_D is the voltage applied to the nanowire, W is the width of the nanowire, L_{stub} is the stub length, and L_{eff} is the stub effective length.

Fig. 2. Quantum device divided in slices for the simulation of quantum transport. The device is connected to two reservoirs.

Fig. 3. The quantum stub transistor with only one open transmission channel. $W = 10nm$, $a = 0.5nm$, $P_W = 19pixels$, $L_{stub} = 11nm$, $M = 1$ (one mode), and $t = 40.52$.

Fig. 4. The quantum stub transistor with four modes. $W = 10nm$, $P_W = 19pixels$, $L_{stub} = 50nm$, $M = 4$ (four modes), and $t = 2.533$.

Fig. 5. Normalized conductance as a function of the gate voltage V_G, for $L_{stub} = 29nm$.

Fig. 6. Normalized conductance as a function of the gate voltage V_G, for $L_{stub} = 50nm$.

Fig. 7. Conductance of the gate-all-around stub transistor as a function of the gate voltage V_G, $L_{stub} = 50nm$ at each side.

Fig. 8. Geometry of the double stub stub transistor, the stub separation is $10nm$, $L_{stub} = 50nm$.

Fig. 9. Conductance of the double stub stub transistor as a function of the gate voltage V_G, the stub separation is $10nm$, $L_{stub} = 50nm$ at each side.

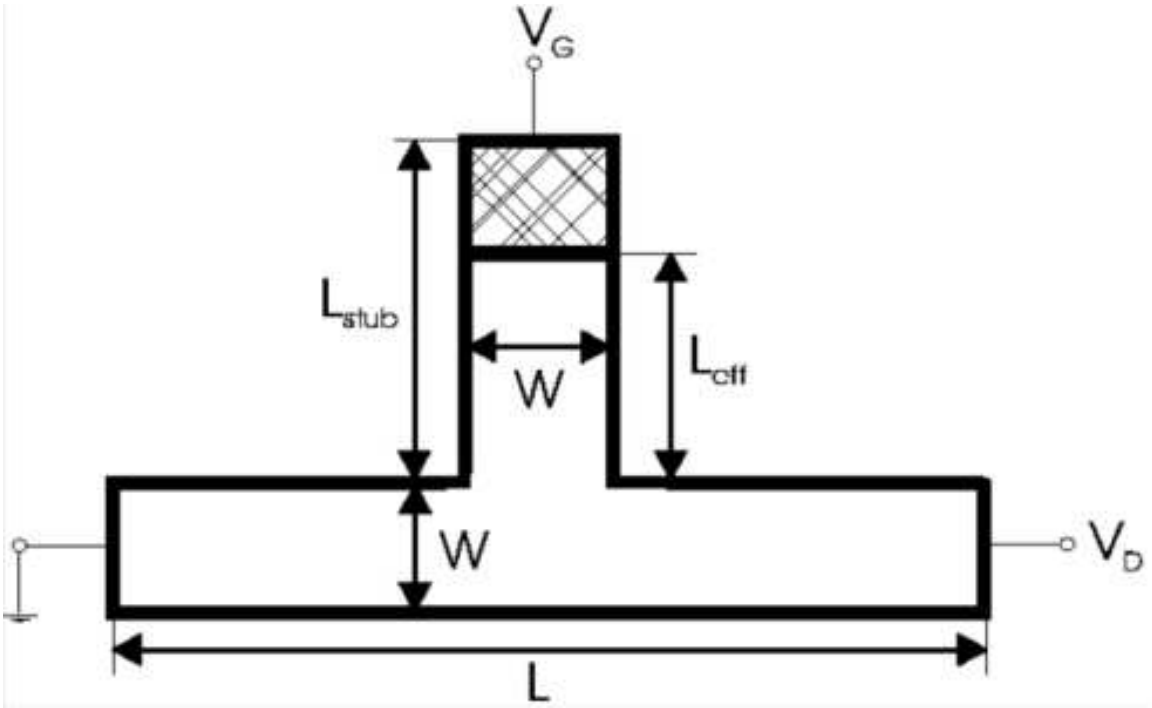


Fig .1 - Guerra and Santos

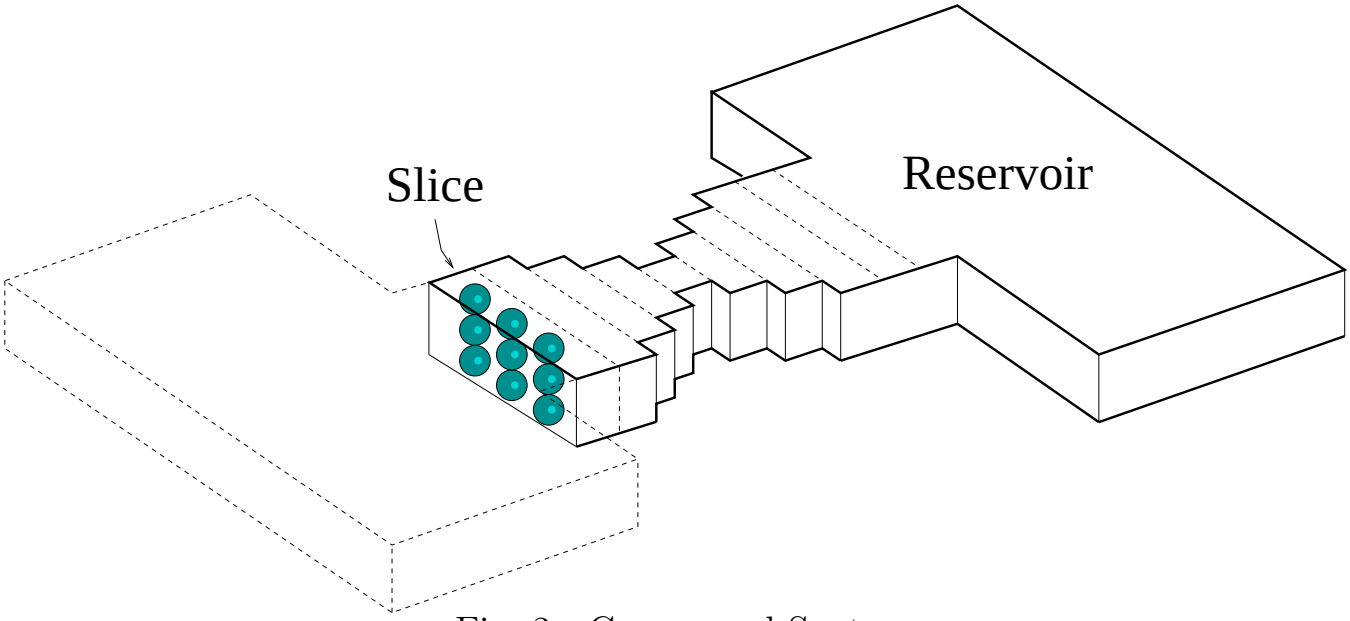
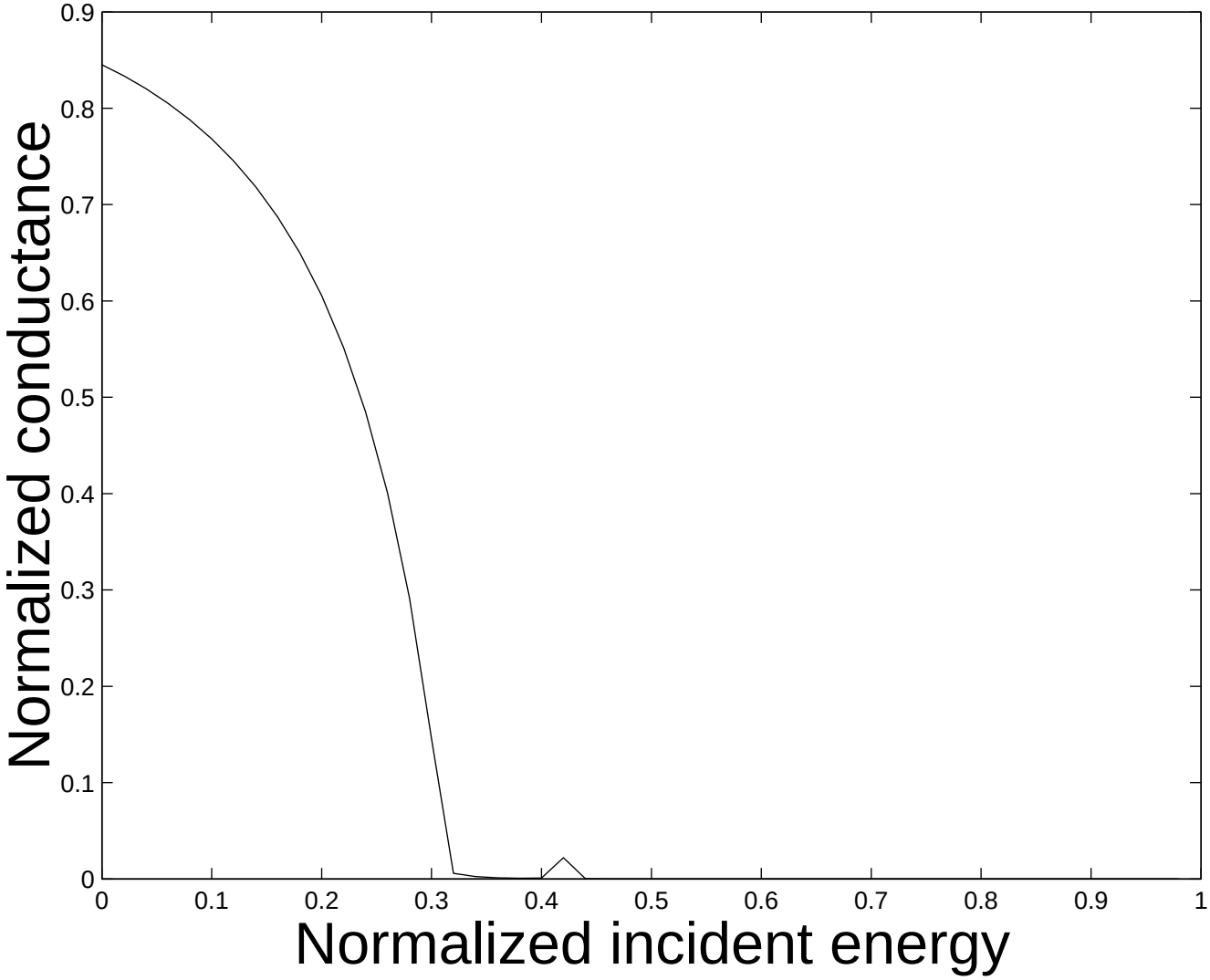


Fig .2 - Guerra and Santos



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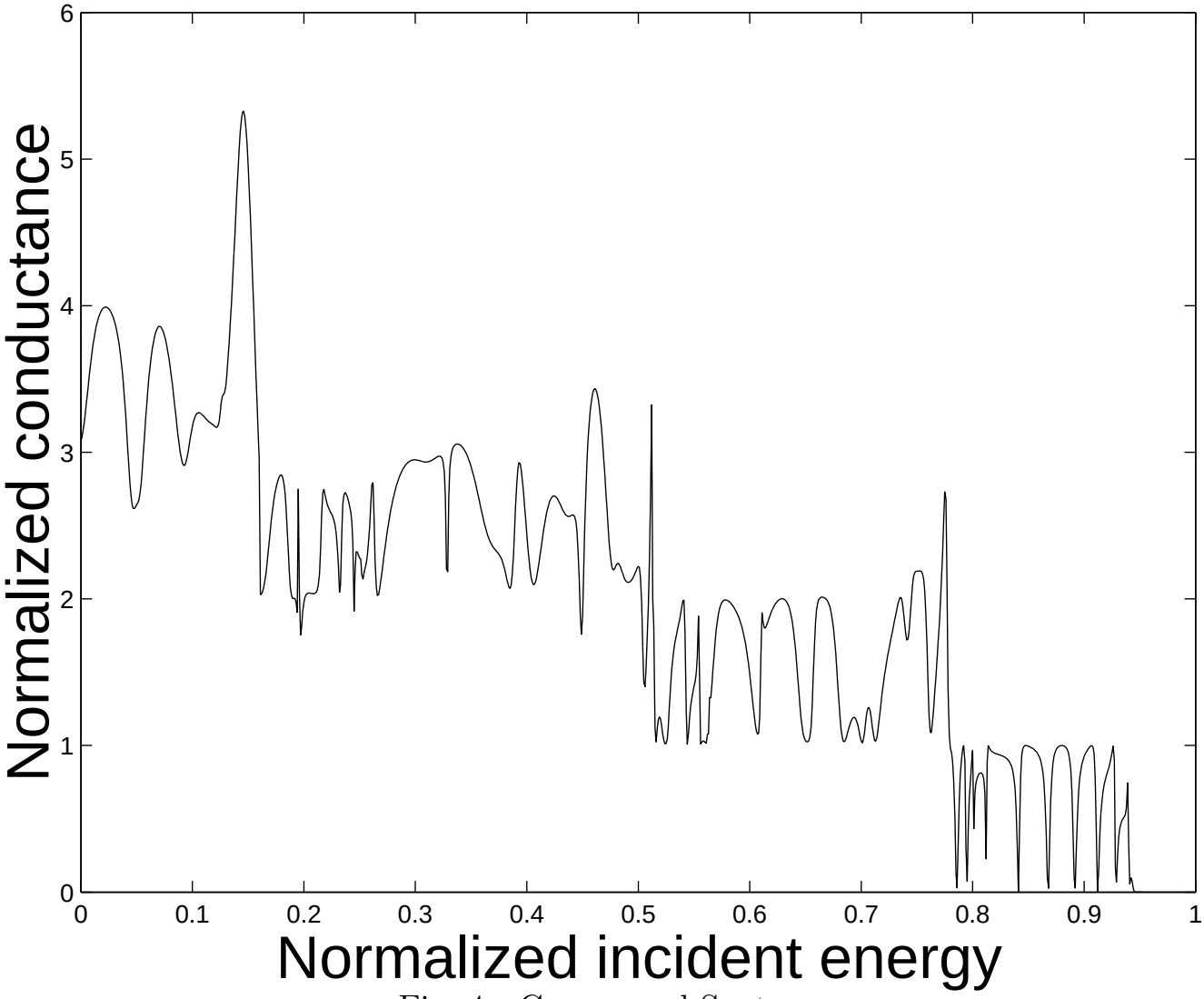

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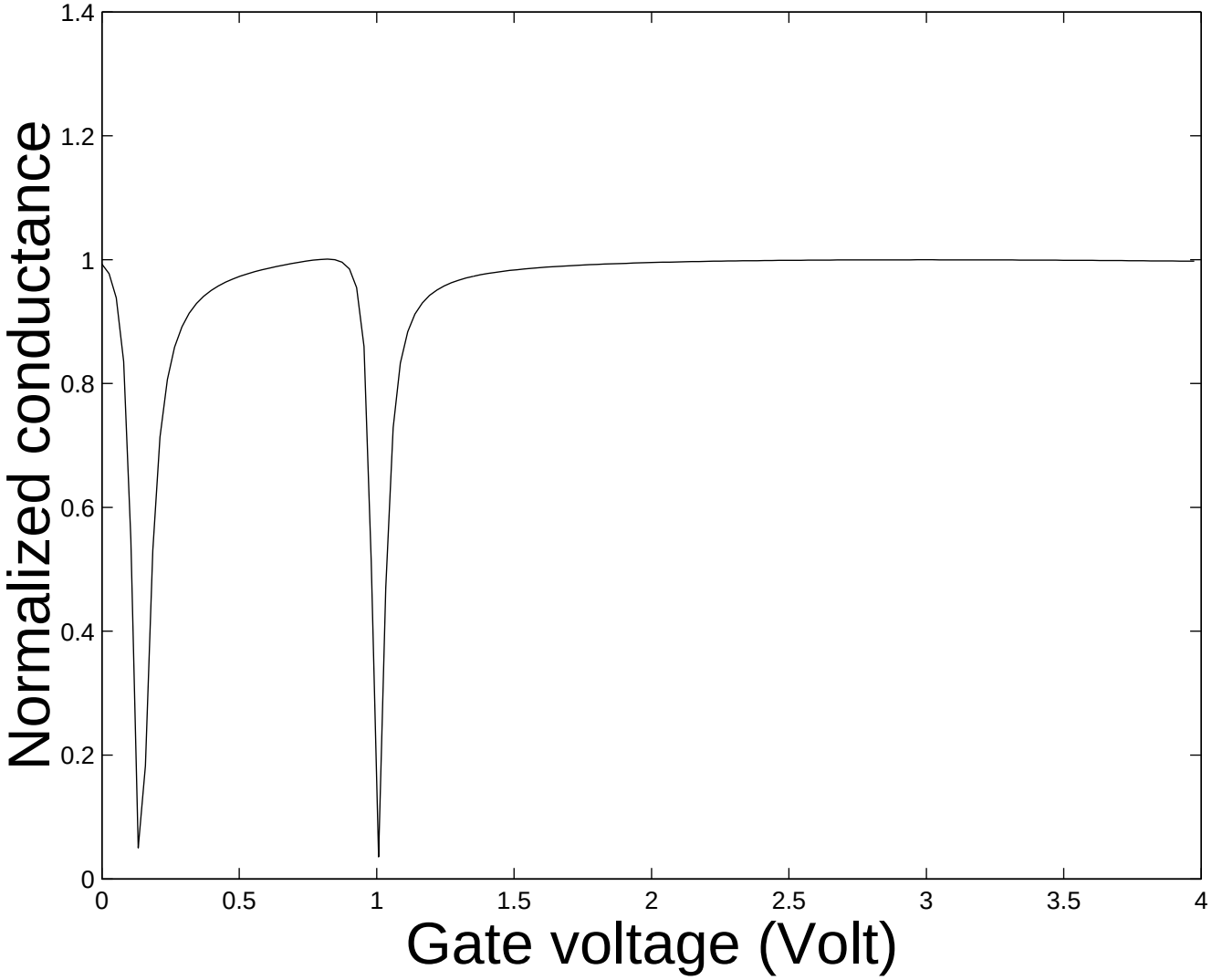

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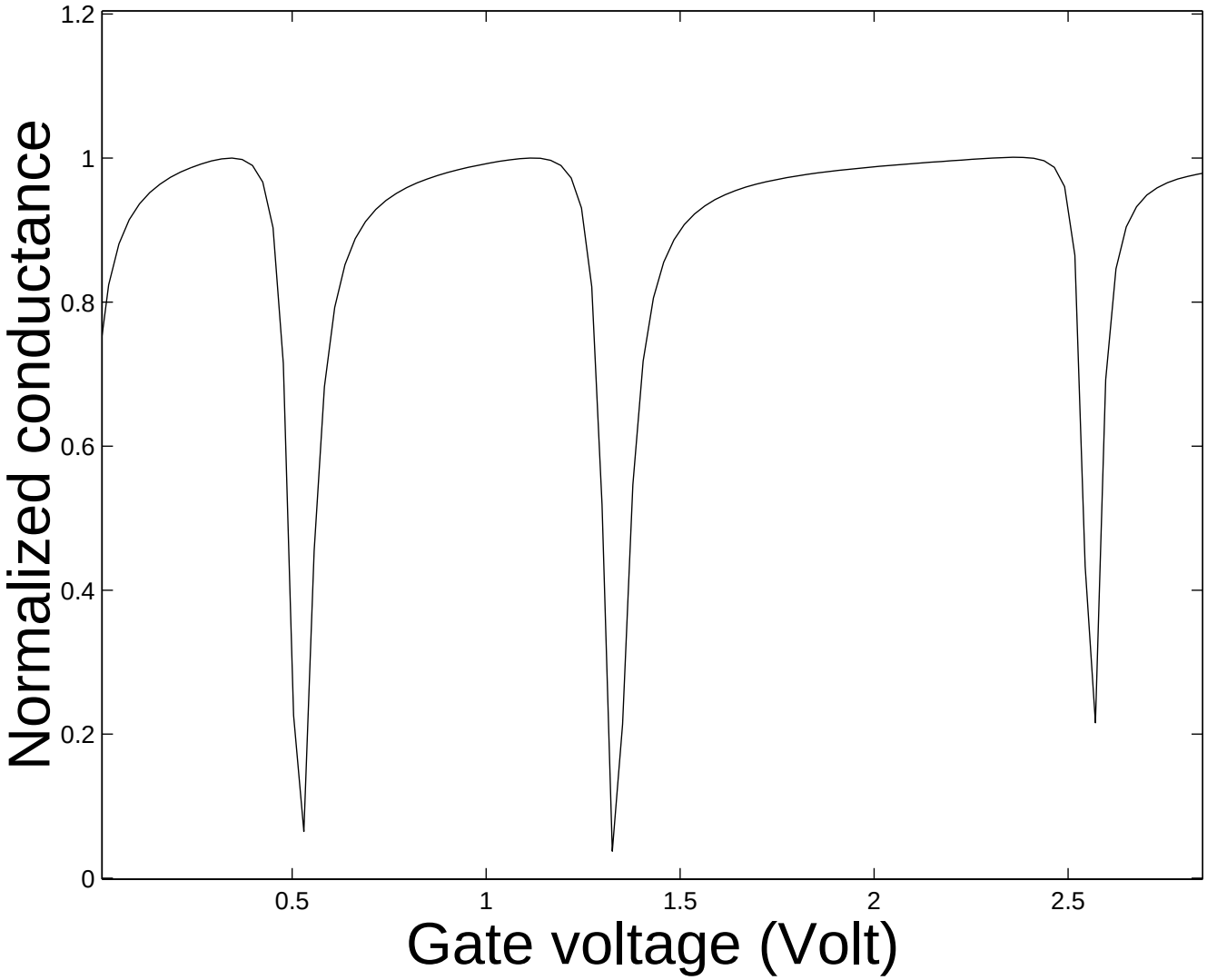

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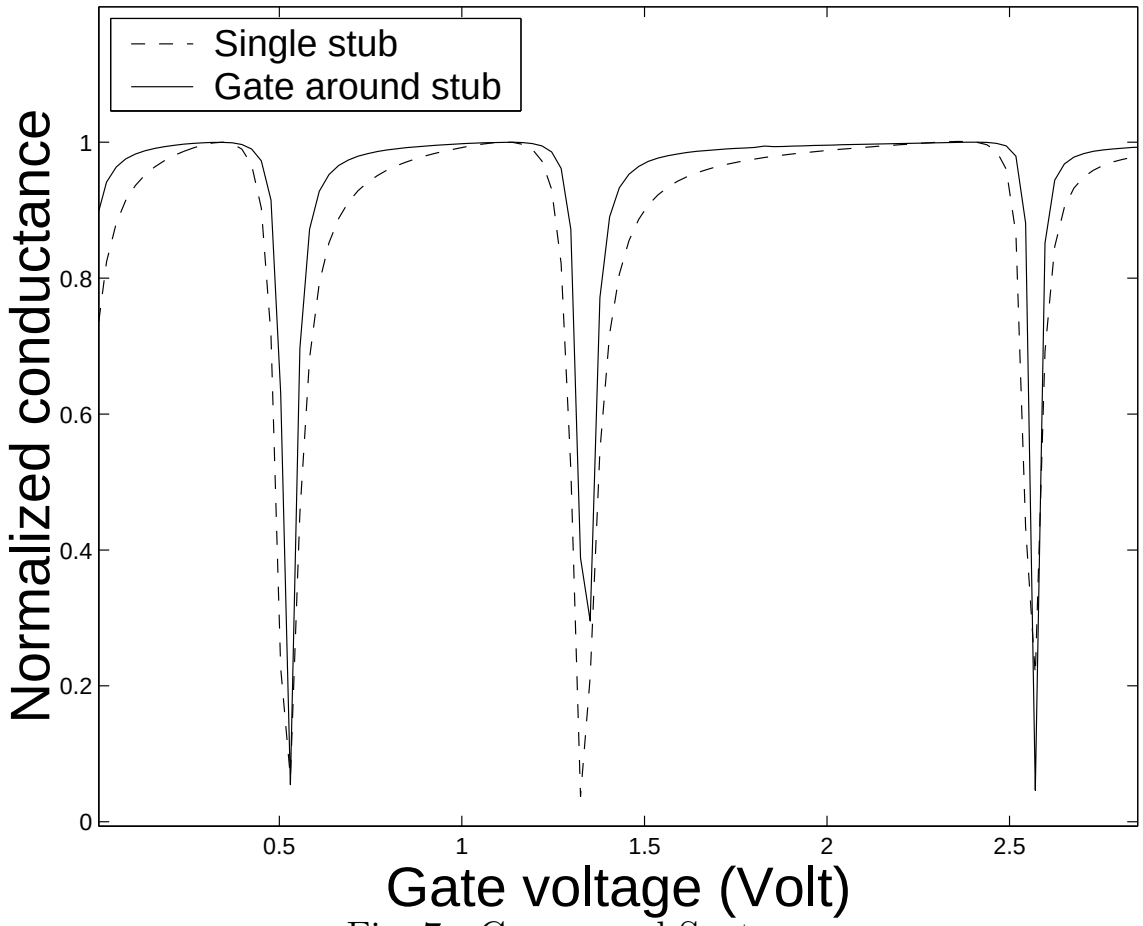

Fig .7 - Guerra and Santos

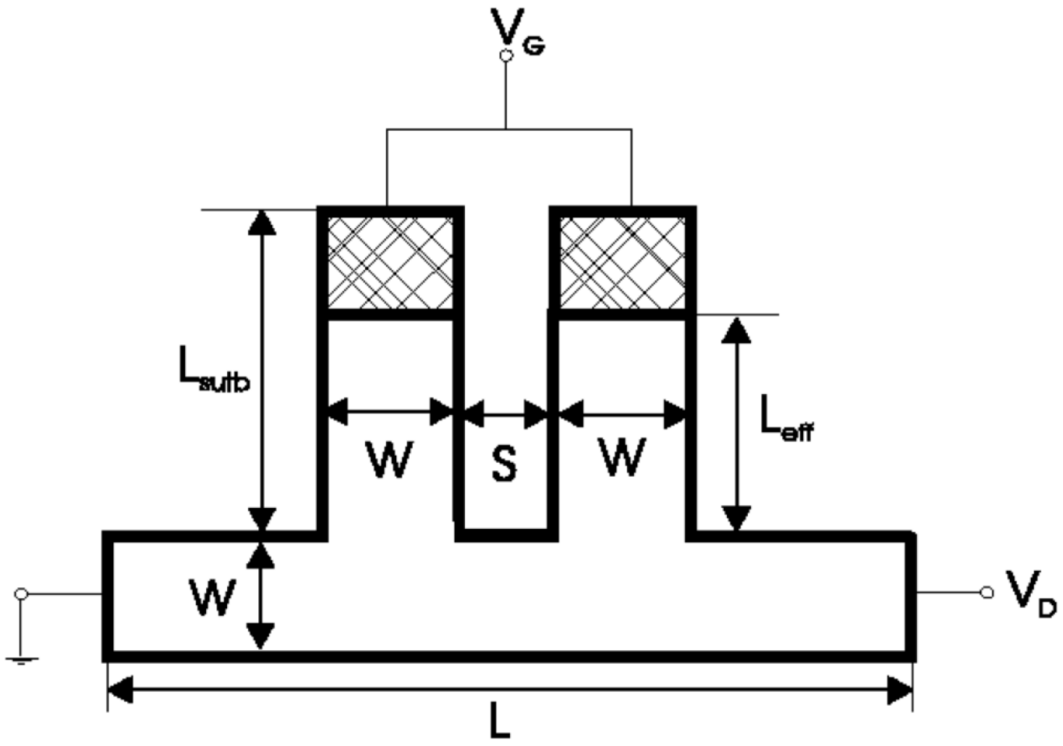

Fig .8 - Guerra and Santos

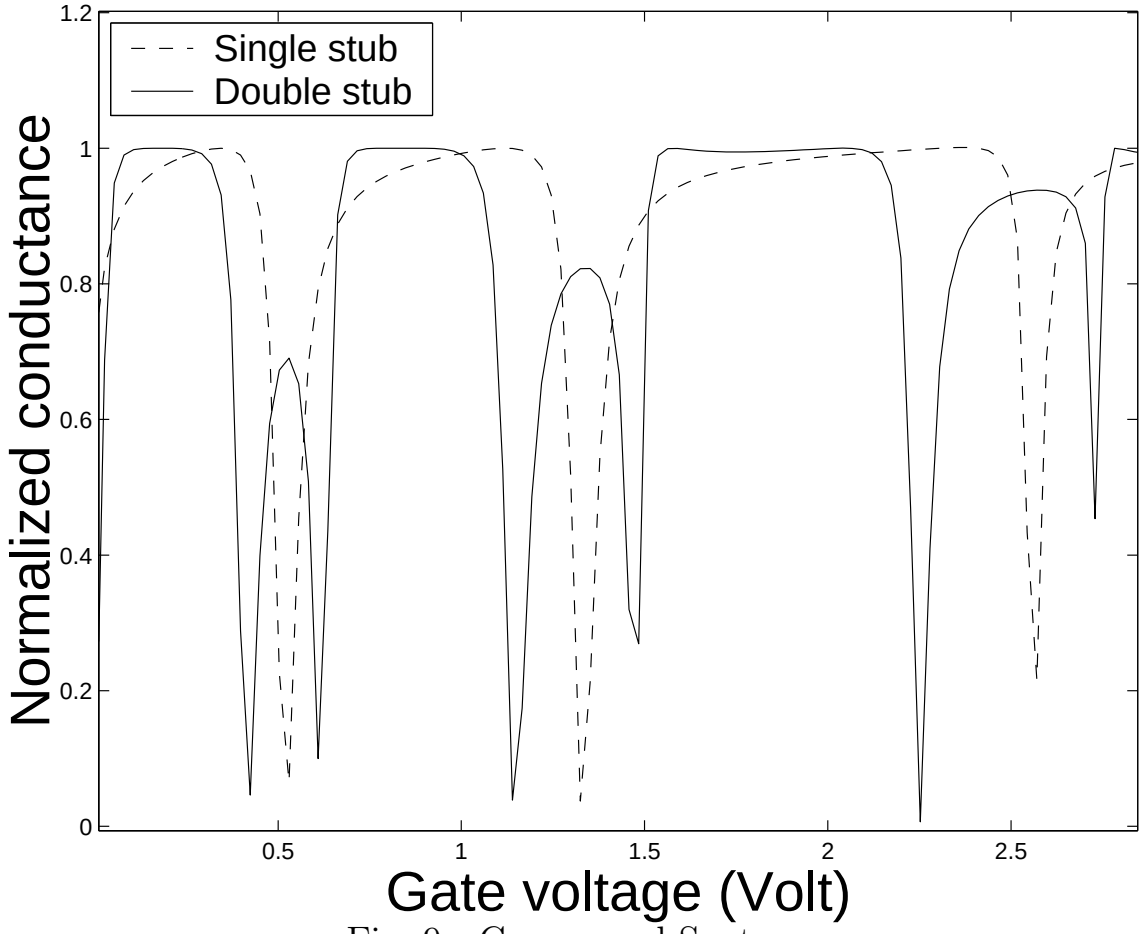

Fig .9 - Guerra and Santos